A NOVEL SINGLE SWITCH-CAPACITOR DAC SAR ADC DESIGN

A THESIS

submitted by

ASHISH S. JOSHI

for the award of the degree

of

MASTER OF SCIENCE
(by RESEARCH)

SCHOOL OF COMPUTING AND ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY MANDI

JULY 2014

To my Family

and

To the Calmness of Himachal

DECLARATION

I hereby declare that the entire work reported in this thesis is the result of investigations carried out by me in School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, under the joint supervision of **Dr. Sanjeev Manhas** and **Dr. Satinder Sharma,** and that it has not been submitted elsewhere for the award of any degree or diploma. In keeping with general practice, due acknowledgments have been made wherever the work described is based on finding of other investigators.

IIT Mandi, Himachal Pradesh,
India
Date:

Ashish Joshi

THESIS CERTIFICATE

This is to certify that the thesis titled **A NOVEL SINGLE SWITCH-CAPACITOR DAC SAR ADC DESIGN,** submitted by **Ashish S. Joshi**, to the Indian Institute of Technology Mandi, for the award of the degree of **Master of Science (by Research)**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other institute or university for the award of any degree or diploma.

EC Dept., IIT Roorkee, Roorkee
Email: samanfec@iitr.ac.in

Dr. Sanjeev Manhas
(Supervisor)

SCEE, IIT Mandi, Mandi
Email: satinder@iitmandi.ac.in

Dr. Satinder Sharma
(Supervisor)

Acknowledgments

First and foremost, I am grateful to the almighty god for blessing me with intelligence, courage and patience, which enabled me to complete this master's thesis successfully.

I would also like to express my gratitude to my parents and family for their unconditional love and strong belief in me. I could not have reached this stage without the freedom, moral and financial support, and the encouragement that they provided me throughout my life. Their concern and caring always extends to the deepest of my heart.

I sincerely would like to thank my research supervisors Dr. Sanjeev Manhas and Dr. Satinder Sharma for their contribution of time, stimulating discussions, patient supervision, constructive criticism and valuable feedback on my work during the entire period of my fruitful association with them. I further wish to extend a vote of thank to Dr. Sudeb Dasgupta for his guidance, helpful suggestions and assistance throughout this work. I consider myself very fortunate for getting the opportunity to learn and work with all of you.

Next, I would like to acknowledge the help and cooperation from Dr. Sukumar Bhattacharya, Dr. Anand Shrivastav, Dr. Bharat Singh Rajpurohit, Dr. Samar Agnihotri and Dr. Venkata Krishnan.

I really enjoyed and cherished the company of my seniors, who turned out to be my close friends here, HVR Mittal, Anshul Sharma and Chander Kant Susheel. Special thanks to all of them for accompanying me to trek, travel and explore the beautiful Himachal.

I am thankful to M. Satish, another senior turned into friend, who made sure I get all the ease and comfort during all the IIT Roorkee trips I made for last two years and Surendra Kumar for providing me with various software support, without which it would have been difficult to reach this level of work within expected time bound.

Lastly, I want to thank all the friends, colleagues and relatives of mine, and also express my apology that I could not mention them personally because of space limitation. I thank all the people who helped me and who didn't helped me while successfully completing this thesis.

Thank you .!

Ashish Joshi

ABSTRACT

Keywords: *SAR ADC, switch-capacitor DAC, RCCM, dynamic comparator*

A switch-capacitor DAC based successive approximation analog to digital converter (SAR-ADC) for sensor-RFID application is presented in this work. To achieve minimum chip area, maximum simplicity is imposed on capacitive DAC; replacing capacitor bank with only one switch-capacitor circuit. The regulated clocked current mirror (RCCM) design is introduced to source (and sink) the stabilized current to (and from) the only capacitor in the circuit. DC reference current from RCCM, charging or discharging the single capacitor in the circuit, is controlled by pulse width modulated signal to realize switch-capacitor DAC. The switch control scheme (SAR control circuit) is built using basic AND gates to generate the control signals for RCCM.

An 8-bit SAR ADC that exhibits a maximum sampling frequency of 100 kHz is designed in 90 nm CMOS technology using Cadence Electronic Design Automation (EDA) tools. Parasitic components extracted from layout are considered in simulation while evaluating the performance of ADC. The use of only one capacitor and reduced transistor count in digital part reduces the silicon area occupied by the ADC to only 0.0098 mm^2. At 100 kS/s and 1 V supply, the converter consumes only 6.75 µW of power and achieves SNDR of 48.68 dB (ENOB of 7.79 bits). The quantization energy (E_Q) for this ADC is calculated to be 305 fJ/conv-step while the evaluated figure of merit (FoM) which takes area occupied by the ADC into consideration is 3.87×10^{20}. The high FoM obtained here shows that the proposed ADC acquires minimal silicon area and has sufficiently low power consumption compared to its counterparts in RFID applications.

Further, the thesis presents a proof of concept for feasibility of FinFET transistors in analog to digital converter design. Inherent suppression of short channel effects, reduced sub-threshold and gate-dielectric leakage, good scalability and ease of integration in analog, digital and RF circuits makes SOI FinFET an important device for mixed signal and system on chip (SoC) solutions. We present an 8 bit, switch-capacitor DAC SAR ADC design in 45 nm SOI double gate FinFET technology and benchmarks the simulation results with similar design in 90 nm bulk CMOS.

Maximum drive is obtained while employing shorted gate (SG) FinFET design for regulated clocked current mirror, sampling unit and SAR control circuitry. The option to separately bias the two gates of FinFET and operate them independently is utilized in comparator design to reduce the power dissipation at higher conversion speed. When compared to 90 nm CMOS ADC, this FinFET based ADC consumes only 2.25 μW of additional power and achieves nine times higher sampling rate.

Contents