Design and Analysis of Front-End Electronics for CMOS Pixel Detectors

Thesis submitted in partial fulfillment of

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DOCTOR OF PHILOSOPHY

by

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Declaration by the Research Scholar

I hereby declare that the entire work embodied in this thesis entitled **"Design and Analysis of Front-End Electronics for CMOS Pixel Detectors"** is the result of investigations carried out by me in the School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India, under the supervision of **Dr. Hitesh Shrimali,** Associate Professor, School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India.

I also declare that it has not been submitted elsewhere for the award of any degree or diploma. In keeping with general practice, due acknowledgments have been made wherever the work described is based on the findings of other investigators. Any omissions that might have occurred due to oversight or error in judgement are regretted.

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Declaration by the Research Advisor

It is certified that the entire work in this thesis entitled **"Design and Analysis of Front-End Electronics for CMOS Pixel Detectors"** has been carried out by **Ms. Indu Yadav,** Enrollment No. D14030, under my supervision and guidance for the degree of Doctor of Philosophy in the School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India.

To the best of my knowledge and belief, present thesis completed by **Ms. Indu Yadav** fulfils the requirements of the Ph.D. ordinance of the Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India. It contains original work of the candidate and no part of it has been submitted elsewhere for any degree or diploma.

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Abstract

With the development in semiconductor industry, silicon pixel detectors have become an important class of sensing devices for imaging applications. In the present era, these detectors cover a broad spectrum of applications viz. photo cameras, bio-medical imaging, X-ray astronomy, space science, radar imaging, and automotive industry. Modern day semiconductor technologies can offer peculiar features to ameliorate the functionality of such systems provided that the foundries allow modifications in the process. High-voltage high-resistive (HV-HR) multi-well process is one of the examples which may benefit the charge collection properties and fill factor percentage. Generally, achieving 100 % fill factor while hosting the signal processing circuitry in a sensor diode, may lead to having noise in terms of fluctuations at the n-well substrate of pMOS transistors. Moreover, the coupling between the pixels via interpixel capacitances introduces crosstalk and may influence the signal charge of the pixel. Therefore, this thesis presents theory, design, implementation, and analysis of a pixel detector with 100 % fill factor. For this, the triple-well STMicroelectronics' BCD8 160 nm technology is used first time as a chosen process foundry to demonstrate the concept and validation of the analysis. The signal processing circuitry consists of a charge sensitive amplifier (CSA), a shaper and a comparator with a cross-corner PVT independent threshold tuning circuit. In this chain of blocks, the CSA is a principal block that defines the performance of the analog front-end. The design of the CSA might be prone to fabrication process variations. Hence, an on-chip corner control circuit is proposed and implemented to obtain the process independent functionality. The interpixel crosstalk becomes significant due to small distance between the pixels in modern detector arrays. The performance of the pixel detectors is also affected by its presence along with the electronic noise. The design process can be optimised and expedited if the noise and crosstalk models for these effects are available. Therefore, the analytical expressions for noise and crosstalk voltages in the analog front-end of pixel detectors are focussed in this research work. Firstly, the noise and crosstalk models are developed for the front-end which has a conventional CSA architecture. Nevertheless, it is observed that the conventional CSA has a limitation with respect to noise. The zero-pole modulation-demodulation with a pulsed reset mechanism is a technique for noise reduction in low rate applications. On the contrary, a continuous reset feedback

network is a viable solution for high rate applications. In this work, the continuous reset zero-pole transformation CSA (ZPT-CSA) has been analysed and a complete transfer function is derived for this CSA. A comparative study is carried out to support the effectiveness of the continuous reset ZPT-CSA over the conventional CSA, in noise reduction. The noise models are also developed for the front-end with the continuous reset ZPT-CSA architecture. The measurement results and circuit simulations are demonstrated to verify the noise and crosstalk models of front-ends with the conventional and the ZPT-CSA, respectively. The designed chip with the conventional CSA architecture is taped-out and characterised using the transient and the noise measurement results. The comparison of noise models with their respective measurement and simulation results show good agreement with each other. Therefore, these noise models can be used for an efficient pixel detector design for the required noise specifications.

Keywords: *Pixel detectors, front-end electronics, electronic noise, interpixel crosstalk, crosstalk modeling and triple-well process.*

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