Multivalent Energy-Efficient CMOS Amplifiers and Data Converters for Signal Processing Applications

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by

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Declaration by the Research Scholar

I hereby declare that the entire work embodied in this thesis entitled **"Multivalent Energy-Efficient CMOS Amplifiers and Data Converters for Signal Processing Applications"** is the result of investigations carried out by me in the School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India, under the joint supervision of **Dr. Satinder Kumar Sharma,** Associate Professor and **Dr. Hitesh Shrimali,** Associate Professor, School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India.

I also declare that it has not been submitted elsewhere for the award of any degree or diploma. In keeping with general practice, due acknowledgments have been made wherever the work described is based on the findings of other investigators. Any omissions that might have occurred due to oversight or error in judgement are regretted.

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It is certified that the entire work in this thesis entitled **"Multivalent Energy-Efficient CMOS Amplifiers and Data Converters for Signal Processing Applications"** has been carried out by **Mr. Ashish Shirish Joshi,** Enrollment No. D14029, under our supervision and guidance for the degree of Doctor of Philosophy in the School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India.

To the best of our knowledge and belief, present thesis completed by **Mr. Ashish Shirish Joshi** fulfils the requirements of the Ph.D. ordinance of the Indian Institute of Technology Mandi, Mandi, Himachal Pradesh, India. It contains original work of the candidate and no part of it has been submitted elsewhere for any degree or diploma.

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Abstract

The advancement of technology has ushered a higher demand for wireless, portable and wearable internet-of-things devices in health monitoring, medical imaging, environmental sensing, communication, agricultural and several other industrial sectors. Analog signal processing (ASP) is an important aspect of various integrated systems that are required in these applications. Miniaturized technology for system design, power dissipation, noise performance, and area consumption are identified as the major challenges for implementing an ASP system. This thesis work addresses the performance-limiting design trade-offs in the amplifier and analog-to-digital converter (ADC) components of the ASP by concentrating on the analysis, design, and implementation of multivalent and configurable circuit techniques that can ameliorate area, noise, and energy efficiencies of the ASP systems.

A low noise chopper amplifier with discrete time parametric amplifier (DTPA) as the signal demodulator is demonstrated using the chip taped-out in a standard 180 nm CMOS technology. The DTPA demodulator enables 8 dB gain enhancement during down-conversion of the chopped signal without compromising on the input impedance and area of the capacitively coupled amplifier in low-frequency data acquisition. Simultaneous concerns between power consumption, unity-gain bandwidth (UGBW) and settling accuracy of an operational transconductance amplifier (OTA) used for medical imaging applications are also addressed herein. A methodology to improve the UGBW and phase margin of a high-speed gain boosted OTA with a positive feedback capacitor across the auxiliary op-amp is presented, and 17 % improvement in 0.01 % settling time is demonstrated based on the presented symbolic analysis. Moreover, a reduced switching activity mode for a successive approximation register (SAR) ADC is developed to minimize power dissipation in the case of multi-sensory applications. Elimination of dispensable switching activity using a temporal reference and maximum design simplicity imposed on the ADC architecture provide easy configurability for the low frequency operation. A secondary switch-and-compare method to generate a supplementary least significant bit is described as well. The technique improves the figure-of-merit of the proof-of-concept SAR ADC with minimal power and area overhead.

Keywords: *Circuit design and analysis, amplifier, data converter, data acquisition front-end.*

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