Alternate High-κ Dielectrics for Next-Generation CMOS Logic and Memory Technology

Submitted in partial fulfillment of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

by

Robin Khosla
(Roll No. D13011)

Supervisor
Dr. Satinder Kumar Sharma

SCHOOL OF COMPUTING & ELECTRICAL ENGINEERING (SCEE)
INDIAN INSTITUTE OF TECHNOLOGY (IIT)-MANDI, MANDI,
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Dedicated to

My Beloved and Respected

Parents

O Dhananjaya, in a devotional mood,
give up attachment to the fruits of karma,
perform your prescribed duties
and become equipoised in success and failure.
Such equanimity is called yoga.

A person who is faithful, who has conquered his senses
and who is devoted to the practice of niskama karma yoga
attains transcendental knowledge.
After attaining transcendental knowledge,
he quickly attains the supreme peace.

---SRIMAD BHAGWAT GITA
(Chapter 2, Sloka 48)
(Chapter 4, Sloka 39)

Declaration by the Research Scholar

I hereby declare that the entire work embodied in this thesis entitled "**Alternate High-κ Dielectrics for Next-Generation CMOS Logic and Memory Technology**" is the result of investigations carried out by me in the School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT)-Mandi, Mandi (H.P), India, under the supervision of **Dr. Satinder Kumar Sharma**, Associate Professor, School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT)-Mandi, Mandi (H.P), India.

I also declare that it has not been submitted elsewhere for any degree or diploma. In keeping with the general practice, due acknowledgments have been made wherever the work described, based on the findings of other investigators. Any omissions that might have occurred due to oversight or error in judgment are regretted.

Place: IIT Mandi

Date:

Signature:

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Robin Khosla
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Declaration by the Research Advisor

It is certified that the thesis work entitled "**Alternate High-κ Dielectrics for Next-Generation CMOS Logic and Memory Technology**" is an original research work done by **Mr. Robin Khosla**, in the School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT) - Mandi, Mandi (H.P), India, under my supervision and guidance for the degree of Doctor of Philosophy in the School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT) - Mandi, Mandi (H.P), India.

To the best of my knowledge and belief, present thesis completed by Mr. Robin Khosla, fulfils the requirements of the Ph.D. ordinance of the Indian Institute of Technology (IIT) - Mandi, Mandi (H.P), India. It contains the original work of candidate himself, and no part of it has been submitted elsewhere for any degree or diploma.

Signature:

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Date:

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Robin Khosla

IIT Mandi, India

Abstract

Incessant scaling of electronic devices in integrated circuits (ICs), since 50 years in accordance with celebrated Moore's Law has revolutionized the semiconductor industry and become an integral part of our day to day life. It has been dictating the exponential growth of chip complexity with decreasing device feature size, and concurrent improvements in circuit speed, memory capacity, and cost per bit. Currently, it is commonly cited that transistors scaling is approaching nano-metric regime and hitting with many fundamental device physics and technology roadblocks. To maintain the higher performance and functionality of scaled logic and memory devices at lower power consumption and affordable costs as required for next generation technology node, the dielectric materials have decreased in thickness from hundreds of nano-meters (nm) to atomistic boundaries. This gives rise to a number of fundamental device physics concerns such as increase in leakage current, power dissipation, channel mobility degradation, decrease in reliability and lifetime for logic and memories devices, as well as process challenges that include integration and optimization of new materials in current semiconductor processing.

Moreover, these issues are not only about the inability of the scaled device performance and reliable operation but also the constraints from the material scientists, economist and technologist point of view. Thus, numerous attempts are being made to introduce new alternate dielectric materials and device structure, especially for logic and memory applications, so that the transistor scaling is not hampered in near future. High-κ dielectrics have emerged as a promising solution for next generation logic and memory applications. Therefore, in this work, the performance, reliability and lifetime of alternate high-κ dielectric materials are methodically investigated by non-destructive, nanoscopic and microscopic techniques for CMOS logic, embedded read only memory and ferroelectric non-volatile memory applications.

For logic devices, erbium oxide (Er_2O_3) shows reasonable dielectric constant, lower leakage current density, higher conduction band offset and Gibbs free energy in contact with silicon, therefore has attracted wide attention of the scientific community. Thus, Er_2O_3 MOS capacitors are fabricated with variation in post-deposition annealing treatment and characterized with various physical, optical and electrical techniques. It reveals that the post deposition furnace annealing (FA) treatment is suitable to obtain high-quality high-κ erbium oxide thin films on active silicon with negligible interfacial oxide formation, low leakage current density, and insignificant hysteresis as desired for CMOS logic applications. The charge trapping and decay analysis of erbium oxide ultrathin films on silicon are systematically investigated by nanoscopic

Kelvin probe force microscopy (KPFM) technique and Er_2O_3 MOS capacitors by microscopic capacitance-voltage (C-V) technique. A simple method is proposed and investigated for trap density estimation using nanoscopic KPFM technique and compared with the conventional macroscopic C-V measurements based trap density estimation method.

Moreover, the continuing advancement in semiconductor technology increasingly requires a significant amount of reliable embedded memory to be integrated with other logic devices circuitry, to take the benefit of on-chip interconnects, higher data rate and also the realization of high-performance futuristic system on chip (SOC) technology. For on-chip embedded memories, bilayer gate stacks have the potential to continue scaling of flash memories to sub-20 nm nodes for short-term by reducing the gate stack thickness and minimize the fundamental cross-coupling capacitance issues among adjacent cells, but the charge trapping mechanism is not well understood and also not well-established, till date. For embedded memories, Al_2O_3 has attracted wide attention because of moderate dielectric constant, high band gap, low-leakage current, high thermal & kinetic stability, few bulk electrically active defects and availability of high-quality thin films formation with atomic layer deposition (ALD) processing. Since SiO_2 layer has the minimum defects, and excellent interface with Si, so direct investigation of charge trapping in high-quality Al_2O_3 or Al_2O_3/SiO_2 interface can be investigated, especially for embedded memory applications. Thus, $Al/Al_2O_3/SiO_2/Si$, MAOS capacitors are fabricated by atomic layer deposition (ALD) and plasma enhanced chemical vapour deposition (PECVD) based Al_2O_3 and SiO_2 thin films, respectively. The fabricated MAOS devices showed high memory window, low leakage current density and high breakdown field that proved the fabricated MAOS structures suitable for on-chip multi-level read only memory applications. The charge trapping properties i.e. trap centroid, trap density and lifetime of bi-layer Al_2O_3/SiO_2 gate stack on Si are investigated by nanoscopic KPFM technique and MAOS capacitors by microscopic techniques. Further, the trap density is estimated systematically by the proposed technique using KPFM at room temperature and compared to the conventional constant current stress based trap density estimation method. Thus, because of high memory window at high voltage the $Al/Al_2O_3/SiO_2/Si$, MAOS system is suitable for high voltage electrically erasable read only type embedded memory applications for bios/code storage.

In the near future to meet the increasing demand of memory density, as a long-term solution, an alternate, and reliable storage mechanism is required, i.e. non-charge storage based emerging

memories, because further scaling of charge stored based memories is hampered by the fewer number of stored electrons that lead to threshold voltage instability due to statistical fluctuations. In this regard, for storage class memories, high-κ based metal-ferroelectric-insulator-semiconductor (MFIS) structure of ferroelectric memories is a prospective contender due to its fast access time, low power consumption, radiation tolerance, non-destructive readout, excellent retention, and endurance time. Among the ferroelectric materials, $PbZrTiO_3$ (PZT) showed high dielectric constant, high remanent polarization, low crystallization temperature and good thermal stability. Also, the titanium oxynitride (TiO_xN_y) has shown exceptional physical and chemical properties, such as high dielectric constant, higher resistance to interfacial oxide formation, and an excellent diffusion barrier. Thus, TiO_xN_y buffer layer is expected as an exceptional candidate for non-volatile ferroelectric memory applications. Therefore, Au/PZT/TiO_xN_y/Si, MFIS capacitors are fabricated using TiO_xN_y buffer and PZT ferroelectric thin films on p-Si by RF-magnetron sputtering and annealed in N_2 ambient. The material characteristics of deposited thin films are investigated by XRD, Micro Raman and AFM analysis that revealed the desired TiO_xN_y rutile, PZT perovskite phases, and high-quality uniform multi-layer interfaces, respectively. Further, the electrical characteristics of Au/PZT/TiO_xN_y/Si, MFIS structures revealed the large memory window, low leakage current, high breakdown strength and exceptional data retention. Moreover, the fabricated devices showed good memory characteristics when subjected to thermal and constant voltage stress that proved the reliability of TiO_xN_y buffer layer for ferroelectric field effect transistor applications.

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Abbreviations

SYMBOL	MEANING
1T	One Transistor
1T-1C	One Transistor - One Capacitor
AFM	Atomic Force Microscopy
A	Area of top gate contact
CMOS	Complementary Metal Oxide Semiconductor
C-F	Capacitance-Frequency
C-V	Capacitance-Voltage
C-T	Capacitance-Time
CVS	Constant Voltage Stress
DRAM	Dynamic Random Access Memory
DRO	Destructive Read Out
ε_o	Permittivity of free space
EEPROM	Electrically Erasable Programmable Read Only Memory
FeFET	Ferroelectric Field Effect Transistor
FeRAM/FRAM	Ferroelectric Random Access Memory
ITRS	International Technology Roadmap for Semiconductors
J-V	Current Density - Voltage
K / ε_r	Dielectric Constant of Insulator/Oxide
KPFM	Kelvin Probe Force Microscopy
MFIS	Metal Ferroelectric Insulator Semiconductor
MFS	Metal Ferroelectric Semiconductor
MIS	Metal Insulator Semiconductor

MISM	Metal Insulator Semiconductor Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MW / ΔW	Memory Window
NDRO	Non-Destructive Read Out
PZT	Lead Zirconate Titanate
RAM	Random Access Memory
ROM	Read Only Memory
SRAM	Static Random Access Memory
SBT	Strontium Bismuth Tantalate
XRD	X-Ray Diffraction

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